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A NOVEL LOW POWER PIPELINED DATAPATH DESIGN USING PARALLELISM HAVING CONSTANT THROUGHPUT

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ABSTRACT

In this paper, we present a novel algorithm to make Pipelined Datapath architecture to be combined with another Datapath module in a Parallel fashion known as Parallel Pipelined datapath. It has the best power saving efficiency of up to 0.1125X as compared to 2.5X, at the cost of decreased throughput from 4X to 1X, while maintaining the same chip area

KEYWORDS: A Novel Low Power Pipelined Datapath Design